U.S.S.N. 10,804,713

Specification Amendments

Please replace paragraph 0025 with the following re-written paragraph:

0025 Fig.'s 2 and 2A illustrate[[s]] a semiconductor device having a fuse according to the present invention.

Please replace paragraph 0026 with the following re-written paragraph:

0026 Fig. 3 illustrates an ~~alternative embodiment~~ expanded view of a semiconductor device having a fuse according to the present invention.

Please replace paragraph 0027 (Specification as numbered) with the following re-written paragraph:

0027 Fig. 2 illustrates a semiconductor device 50 with portions broken away according to the present invention. Figure 2 shows portions of the dual damascene structures of the fuse and

guard ring structure 34 in more detail including the guard ring 34, e.g., taken in a cross section taken along 'A' as shown in Figure 3 (note that as explained above the guard ring (dummy damascene structures) completely surrounds the fuse structure). Figure 2A shows the same cross section as Figure 3 in more detail, but without the guard ring 34. The semiconductor device 50 may include a base portion (not shown) with discrete devices formed therein. The semiconductor device 50 may also includes an oxide or low dielectric material 52 including a number of discrete semiconductor structures (not shown) formed therein. A multilayer structure may be formed over the oxide or low dielectric material 52 including a plurality of dielectric layers 56 which may be silicon dioxide, or may be a low dielectric material such as polyimide nanoforms or porous glasses. An etch-stop layer 54 such as silicon nitride may be positioned between adjacent layers of dielectric material. A damascene structure 58 is provided in the dielectric material and includes at least a first (first from the topmost metallization layer) metallization layer 60, a plug 62 and a topmost (second) metallization layer 64 of the damascene structures connecting to the fuse (66) ~~which may be the top metallization layer~~. As shown in Figure 2, the guard ring (34) may include a metallization structure e.g., 64A above the fuse 66 to completely surround the fuse cavity/window (30).

The top metallization layer ~~62~~ 64 may have a thickness of about 9000 angstroms or more. A fuse 66 is formed on the topmost metallization layer 64. Preferably the fuse is aluminum material formed at a thickness of about 1000-7000 angstroms and preferably 3500 angstroms. The fuse may be formed by an additional masking step using a patterned photoresist layer with an opening therein through which the aluminum may be deposited on top of the top metallization layer 64 by electroplating, screening or other methods known to those skilled in the art. An additional passivation layer 68 may be provided over the multilayer structures and may be a single layer or a layer of plasma enhanced silicon nitride to a thickness of about 750 angstroms and a layer of plasma enhanced oxide to a thickness of about 4000 angstroms. Additional passivation layers 72, 74 may also be provided and may be a layer of plasma enhanced oxide to a thickness of about 4000 angstroms and layer of plasma enhanced silicon nitride to a thickness of about 6000 angstroms. A fuse window ~~76~~ 30 is provided through the passivation layers down to the fuse passivation layer 68. The fuse 66 may be blown by energizing the fuse with a laser through the fuse passivation layer 68. Preferably when the dielectric layers 52, 56 are a low dielectric material, a laser beam is utilized to blow the fuse. The low dielectric material layers 52, 56 may have a dielectric

constant k ranging from 2.0-3.6 and preferably from 2.2-3.0. The combination of a low dielectric and a thick top metal layer such as a copper damascene structure with a low-k dielectric increases the chance of having lower corner cracks and copper fuse residue due to the low-k dielectric softness. Lower corner cracking may produce unclean link removal and damage to the circuit. Consequently, metal links are cut more effectively at lower nominal energies and less likely to have lower corner cracking beneath the fuse link.

Please replace paragraph 0028 with the following re-written paragraph:

[0028] Fig. 3 illustrates a semiconductor device 10 having a fuse 12 according to the present invention in an expanded view, but without showing the various dielectric layers as shown in Figures 2 and 2A. The structure shown in Fig. 3 is similar to the prior art structure shown in Fig. 1 with the exception that the fuse 12 includes a first layer 78 of copper lines and a second layer 80 of aluminum. Again, a thin layer of dielectric 32 overlies the fuse 12. The use of the aluminum layer 80 reduces the chance of the copper from forming oxides after the

fuse is blown.